

## High-Voltage Switchmode Regulator

### FEATURES

- 10- to 120-V Input Range
- Current-Mode Control
- On-Chip 200-V, 5- $\Omega$  MOSFET Switch
- SHUTDOWN and RESET
- High Efficiency Operation (>80%)
- Internal Start-Up Circuit
- Internal Oscillator (1 MHz)

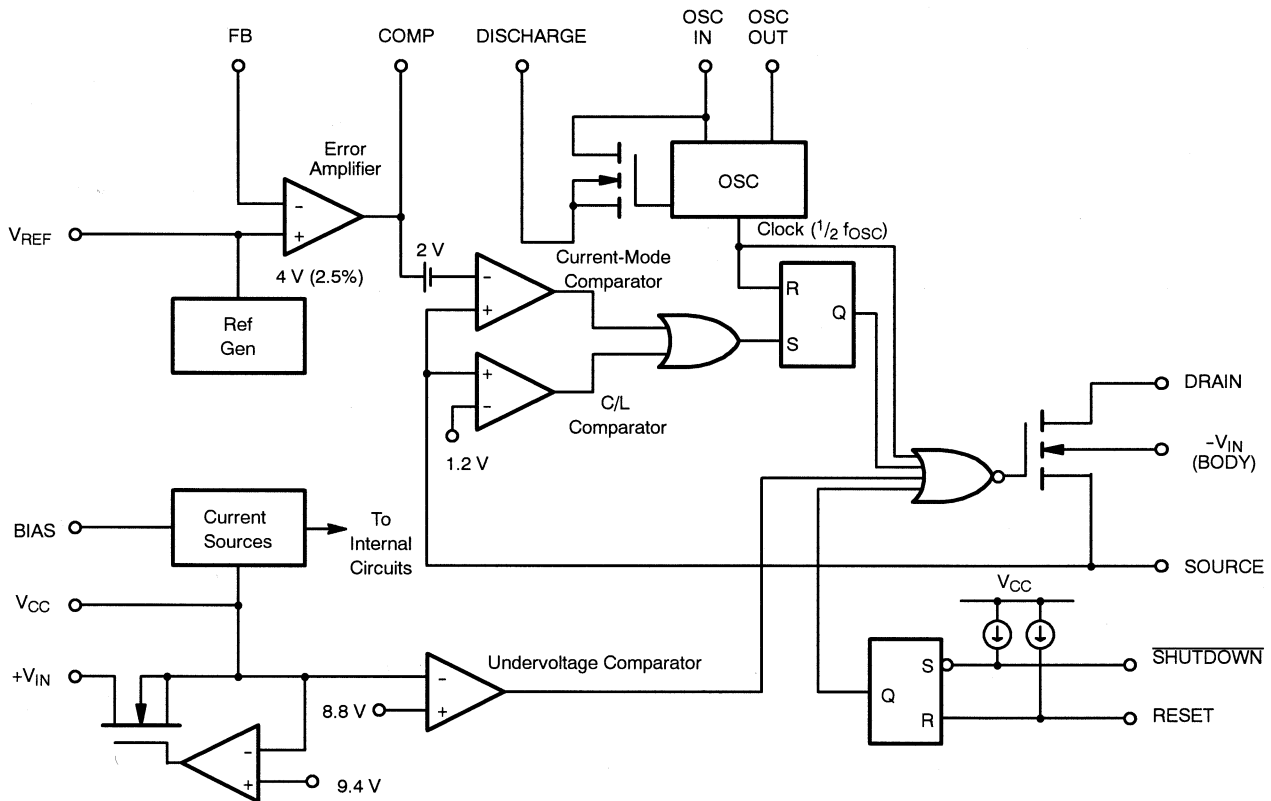
### DESCRIPTION

The Si9104 high-voltage switchmode regulator is a monolithic BiC/DMOS integrated circuit which contains most of the components necessary to implement a high-efficiency dc-to-dc converter up to 3 watts. It can either be operated from a low-voltage dc supply, or directly from a 10- to 120-V unregulated dc power source.

This device may be used with an appropriate transformer to implement most single-ended isolated power converter topologies (i.e., flyback and forward).

The Si9104 is available in a 16-pin wide-body SOIC and is specified over the D suffix (-40 to 85°C) temperature range.

### FUNCTIONAL BLOCK DIAGRAM





## ABSOLUTE MAXIMUM RATINGS

Voltages Referenced to  $-V_{IN}$  ( $V_{CC} < +V_{IN} + 0.3\text{ V}$ )

$V_{CC}$ .....	15 V
$+V_{IN}$ .....	120 V
$V_{DS}$ .....	200 V
$I_D$ (Peak) (300 $\mu\text{s}$ pulse, 2% duty cycle) .....	2 A
$I_D$ (rms) .....	250 mA
Logic Inputs (RESET, SHUTDOWN, OSC IN) ..	-0.3 V to $V_{CC} + 0.3\text{ V}$
Linear Inputs (FEEDBACK, SOURCE) .....	-0.3 V to 7 V
HV Pre-Regulator Input Current (continuous) .....	3 mA
Storage Temperature .....	-65 to 125°C

Operating Temperature .....

Junction Temperature ( $T_J$ ) .....

Power Dissipation (Package)<sup>a</sup>

16-Pin Plastic Wide-Body SOIC<sup>b</sup> .....

Thermal Impedance ( $\theta_{JA}$ )

16-Pin Plastic Wide-Body SOIC .....

Notes

a. Device mounted with all leads soldered or welded to PC board.

b. Derate 7.2 mW/°C above 25°C.

RECOMMENDED OPERATING RANGE

Voltages Referenced to  $-V_{IN}$

$V_{CC}$ .....	10 V to 13.5 V
$+V_{IN}$ .....	10 V to 120 V
$f_{OSC}$ .....	.40 kHz to 1 MHz

$R_{OSC}$  .....

Linear Inputs .....

Digital Inputs .....

SPECIFICATIONS <sup>a</sup>							
Parameter	Symbol	Test Conditions Unless Otherwise Specified DISCHARGE = $-V_{IN} = 0\text{ V}$ , $V_{CC} = 10\text{ V}$ $+V_{IN} = 48\text{ V}$ , $R_{BIAS} = 390\text{ k}\Omega$ $R_{OSC} = 330\text{ k}\Omega$	Limits D Suffix -40 to 85°C				Unit
			Temp <sup>b</sup>	Min <sup>d</sup>	Typ <sup>c</sup>	Max <sup>d</sup>	
<b>Reference</b>							
Output Voltage	$V_R$	OSC IN = $-V_{IN}$ (OSC Disabled) $R_L = 10\text{ M}\Omega$	Room Full	3.92 3.85	4.0	4.08 4.15	V
Output Impedance <sup>e</sup>	$Z_{OUT}$		Room	15	30	45	k $\Omega$
Short Circuit Current	$I_{SREF}$	$V_{REF} = -V_{IN}$	Room	70	100	130	$\mu\text{A}$
Temperature Stability <sup>e</sup>	$T_{REF}$		Full		0.25	1.0	mV/°C
Long Term Stability <sup>e</sup>		$t = 1000\text{ hrs.}$ , $T_A = 125^\circ\text{C}$	Room		5	25	mV
<b>Oscillator</b>							
Maximum Frequency <sup>e</sup>	$f_{MAX}$	$R_{OSC} = 0$	Room	1	3		MHz
Initial Accuracy	$f_{OSC}$	$R_{OSC} = 330\text{ k}\Omega^f$	Room	80	100	120	kHz
		$R_{OSC} = 150\text{ k}\Omega^f$	Room	160	200	240	
Voltage Stability	$\Delta f/f$	$\Delta f/f = f(13.5\text{ V}) - f(10\text{ V}) / f(10\text{ V})$	Room	4	10	15	%
Temperature Coefficient <sup>e</sup>	$T_{OSC}$		Full		200	500	ppm/°C
<b>Error Amplifier</b>							
Feedback Input Voltage	$V_{FB}$	FB Tied to COMP OSC IN = $-V_{IN}$ (OSC Disabled)	Room	3.96	4.00	4.04	V
Input BIAS Current	$I_{FB}$	OSC IN = $-V_{IN}$ , $V_{FB} = 4\text{ V}$	Room		25	500	nA
Input OFFSET Voltage	$V_{OS}$	OSC IN = $-V_{IN}$ (OSC Disabled)	Room		$\pm 15$	$\pm 40$	mV
Open Loop Voltage Gain <sup>e</sup>	$A_{VOL}$		Room	60	80		dB
Unity Gain Bandwidth <sup>e</sup>	BW		Room	0.7	1		MHz
Dynamic Output Impedance <sup>e</sup>	$Z_{OUT}$		Room		1000	2000	$\Omega$
Output Current	$I_{OUT}$		Source ( $V_{FB} = 3.4\text{ V}$ )	Room		-2.0	-1.4
		Sink ( $V_{FB} = 4.5\text{ V}$ )	Room	0.12	0.15		
Power Supply Rejection	PSRR	$10\text{ V} \leq V_{CC} \leq 13.5\text{ V}$	Room	50	70		dB

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SPECIFICATIONS <sup>a</sup>							
Parameter	Symbol	Test Conditions Unless Otherwise Specified DISCHARGE = -V <sub>IN</sub> = 0 V, V <sub>CC</sub> = 10 V +V <sub>IN</sub> = 48 V, R <sub>BIAS</sub> = 390 kΩ R <sub>OSC</sub> = 330 kΩ	Limits D Suffix -40 to 85°C				Unit
			Temp <sup>b</sup>	Min <sup>d</sup>	Typ <sup>c</sup>	Max <sup>d</sup>	
<b>Current Limit</b>							
Threshold Voltage	V <sub>SOURCE</sub>	R <sub>L</sub> = 100 Ω from DRAIN to V <sub>CC</sub> , V <sub>FB</sub> = 0 V	Room	1.0	1.2	1.4	V
Delay to Output	t <sub>d</sub>	R <sub>L</sub> = 100 Ω from DRAIN to V <sub>CC</sub> V <sub>SOURCE</sub> = 1.5 V, See Figure 1.	Room		100	200	ns
<b>Pre-Regulator/Start-Up</b>							
Input Voltage	+V <sub>IN</sub>	I <sub>IN</sub> = 10 μA	Room	120			V
Input Leakage Current	+I <sub>IN</sub>	V <sub>CC</sub> ≥ 10 V	Room			10	μA
Pre-Regulator Start-Up Current	I <sub>START</sub>	Pulse Width ≤ 300 μs, V <sub>CC</sub> = 7 V	Room	8	15		mA
V <sub>CC</sub> Pre-Regulator Turn-Off Threshold Voltage	V <sub>REG</sub>	I <sub>PRE-REGULATOR</sub> = 10 μA	Room	7.8	9.4	9.8	V
Undervoltage Lockout	V <sub>UVLO</sub>	R <sub>L</sub> = 100 Ω from DRAIN to V <sub>CC</sub> See Detailed Description	Room	7.0	8.8	9.3	
V <sub>REG</sub> - V <sub>UVLO</sub>	V <sub>DELTA</sub>		Room	0.3	0.6		
<b>Supply</b>							
Supply Current	I <sub>CC</sub>		Room	0.45	0.6	1.0	mA
Bias Current	I <sub>BIAS</sub>		Room	10	15	20	μA
<b>Logic</b>							
SHUTDOWN Delay <sup>e</sup>	t <sub>SD</sub>	V <sub>SOURCE</sub> = -V <sub>IN</sub> , See Figure 2.	Room		50	100	ns
SHUTDOWN Pulse Width <sup>e</sup>	t <sub>SW</sub>	See Figure 3.	Room	50			
RESET Pulse Width <sup>e</sup>	t <sub>RW</sub>		Room	50			
Latching Pulse Width <sup>e</sup> SHUTDOWN and RESET Low	t <sub>LW</sub>		Room	25			
Input Low Voltage	V <sub>IL</sub>			Room			2.0
Input High Voltage	V <sub>IH</sub>		Room	8.0			
Input Current Input Voltage High	I <sub>IH</sub>	V <sub>IN</sub> = V <sub>CC</sub>	Room		1	5	μA
Input Current Input Voltage Low	I <sub>IL</sub>	V <sub>IN</sub> = 0 V	Room	-35	-25		
<b>MOSFET Switch</b>							
Breakdown Voltage	V <sub>BR(DSS)</sub>	I <sub>DRAIN</sub> = 100 μA	Full	200	220		V
Drain-Source On-Resistance <sup>g</sup>	r <sub>DS(on)</sub>	I <sub>DRAIN</sub> = 100 mA	Room		3	5	Ω
Drain Off Leakage Current	I <sub>DSS</sub>	V <sub>DRAIN</sub> = 150 V	Room		5	10	μA
Drain Capacitance <sup>e</sup>	C <sub>DS</sub>		Room		35		pF

Notes

- a. Refer to PROCESS OPTION FLOWCHART for additional information.
- b. Room = 25°C, Cold and Hot = as determined by the operating temperature suffix.
- c. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
- d. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
- e. Guaranteed by design, not subject to production test.
- f. C<sub>STRAY</sub> @ OSC IN ≤ 5 pF.
- g. Temperature coefficient of r<sub>DS(on)</sub> is 0.75% per °C, typical.

TIMING WAVEFORMS

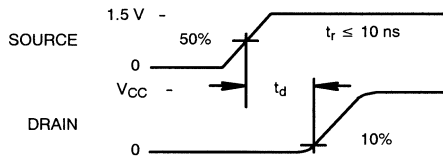


FIGURE 1.

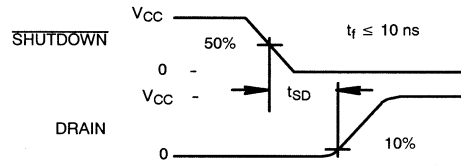


FIGURE 2.

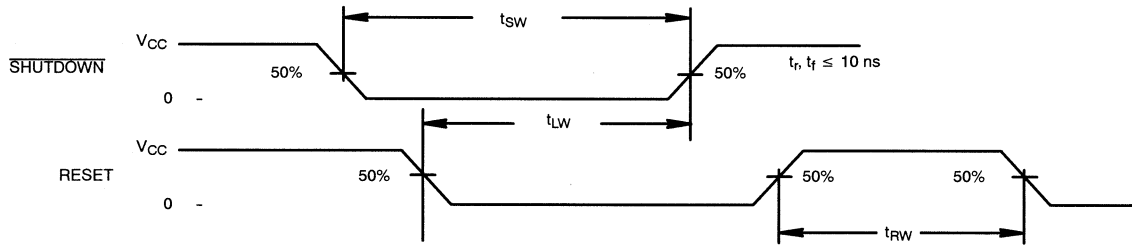


FIGURE 3.

TYPICAL CHARACTERISTICS

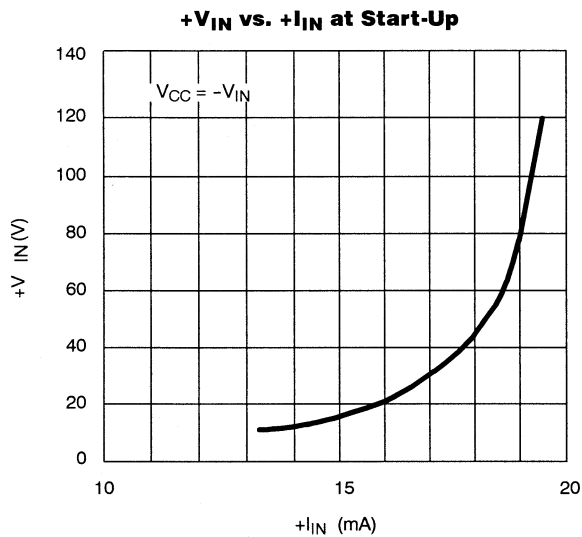


FIGURE 4.

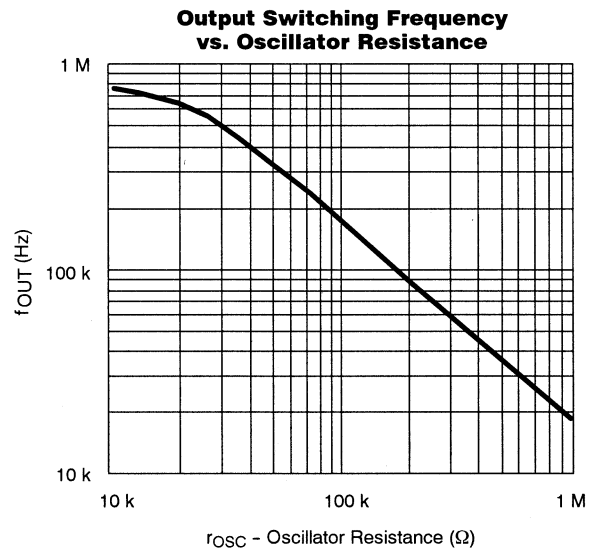
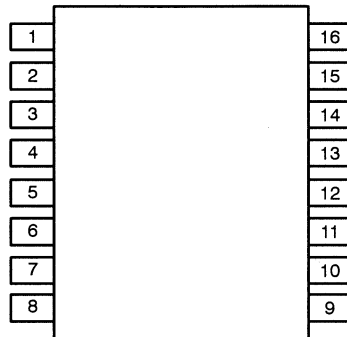


FIGURE 5.

## PIN CONFIGURATIONS

**SO-16  
(Wide-Body)**


Top View

Order Number: Si9104DW

PIN DESCRIPTION			
Function	Pin Number		
	14-Pin Plastic DIP	16-Pin SOIC	20-Pin PLCC
SOURCE	4	1	7
-V <sub>IN</sub>	5	2	8
V <sub>CC</sub>	6	4	9
OSC <sub>OUT</sub>	7	5	10
OSC <sub>IN</sub>	8	6	11
DISCHARGE	9	7	12
V <sub>REF</sub>	10	8	14
SHUTDOWN	11	9	16
RESET	12	10	17
COMP	13	11	18
FB	14	12	20
BIAS	1	13	2
+V <sub>IN</sub>	2	14	3
DRAIN	3	16	5
NC		3, 15	1, 4, 6, 13, 15, 19




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